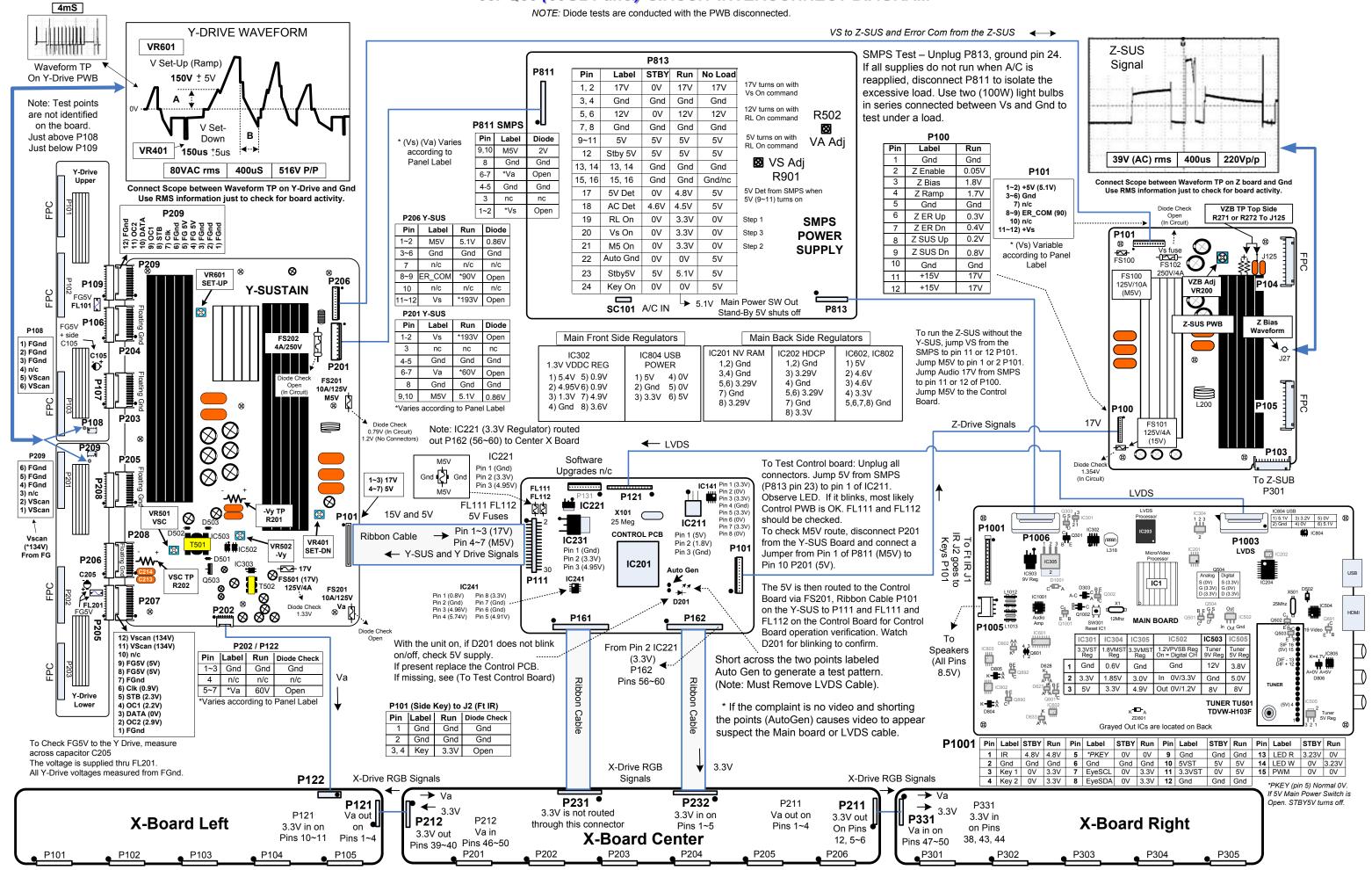
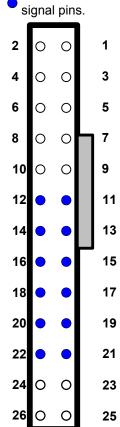
50PQ30 (50G2 Panel) CIRCUIT INTERCONNECT DIAGRAM



50PQ30 LVDS P1003 **WAVEFORMS**

Connector P1003 Configuration

indicates signal pins.



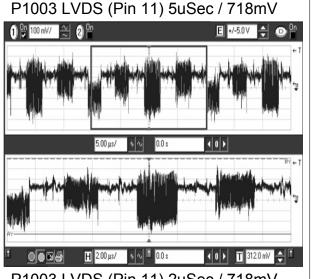
NOTE: LVDS P1003 Information

There are actually 12 pins carrying Video 2 pins are carrying clock signals (17 and 18) to the Control board. With high activity video, pins 21 and 22 would have signals present.

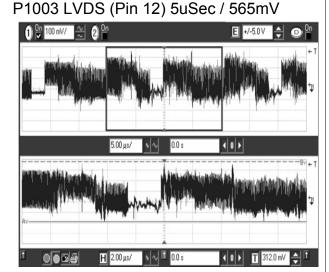
WAVEFORMS:

Waveforms taken using SMTP Color Bar input. All readings give their Time Base related to scope settings.

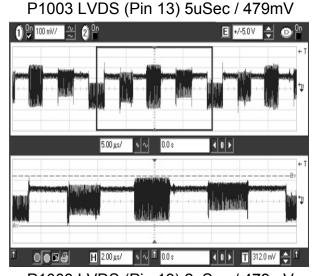
All waveforms taken from the P1003.



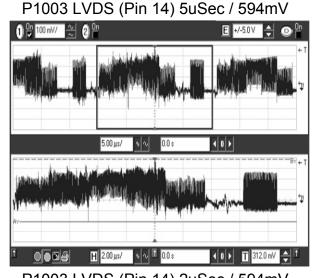
P1003 LVDS (Pin 11) 2uSec / 718mV



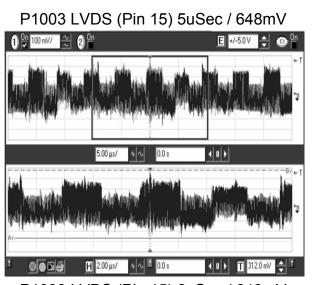
P1003 LVDS (Pin 12) 2uSec / 565mV



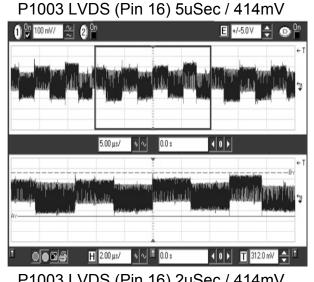
P1003 LVDS (Pin 13) 2uSec / 479mV



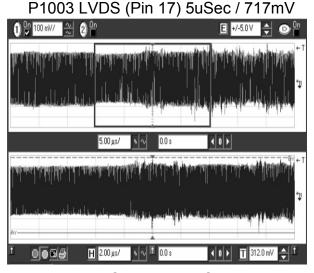
P1003 LVDS (Pin 14) 2uSec / 594mV



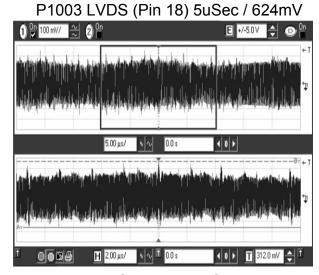
P1003 LVDS (Pin 15) 2uSec / 648mV



P1003 LVDS (Pin 16) 2uSec / 414mV

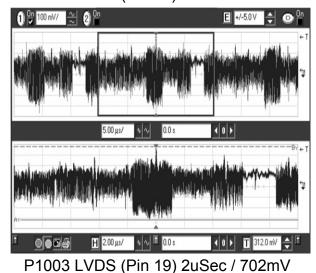


P1003 LVDS (Pin 17) 2uSec / 717mV

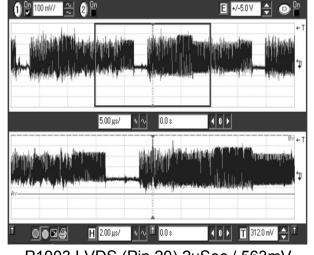


P1003 LVDS (Pin 18) 2uSec / 624mV

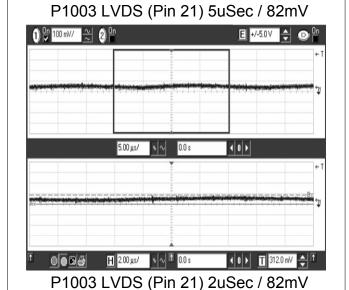




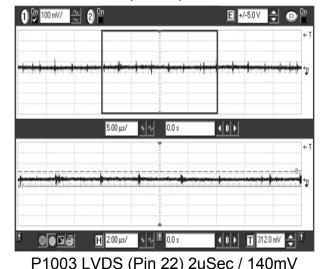
P1003 LVDS (Pin 20) 5uSec / 563mV



P1003 LVDS (Pin 20) 2uSec / 563mV

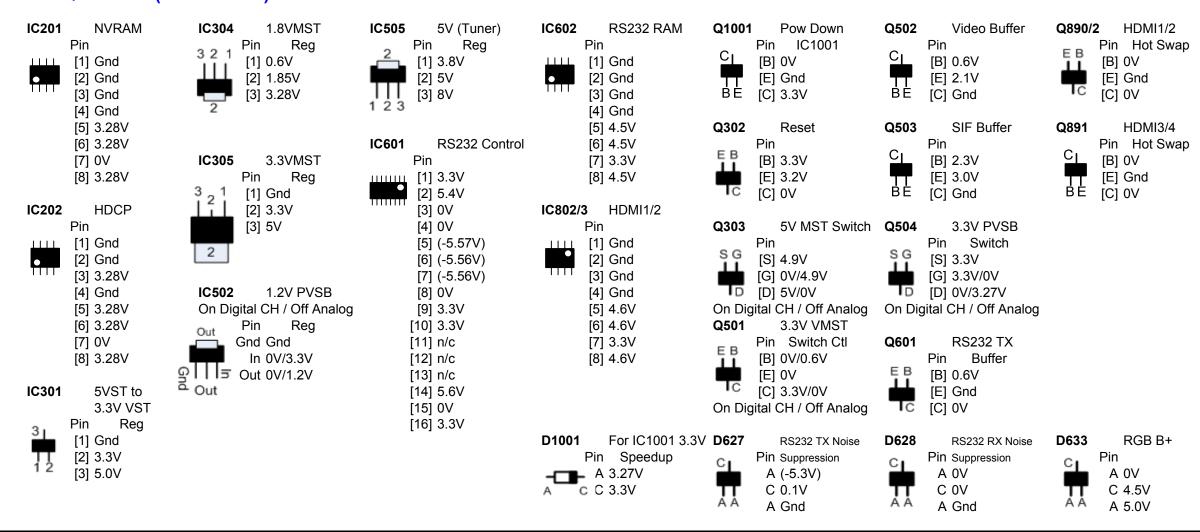


P1003 LVDS (Pin 22) 5uSec / 140mV



P1003 LVDS (Pin 22) 2uSec / 140mV

50PQ30 MAIN (BACK SIDE) SIMICONDUCTORS



50PQ30 MAIN (FRONT SIDE) SIMICONDUCTORS

